

# RFCMOS Case Study: Orca Systems' 1st-pass Functional Silicon Success with Fujitsu CMOS 90nm Technology

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ORCA Systems, Inc.

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## Introduction

The advent of advanced CMOS as the technology of choice for RF system implementation has introduced new challenges to the development flow of highly integrated products. These next-generation challenges have increased the need for validated PDK design environments in order to accurately assess circuit performance across all phases of product development. Among these new challenges, the need to achieve first-pass functional silicon is critical since development cycle reductions improve time-to-market and minimize development costs. To this end, Fujitsu has developed a PDK that directly addresses these challenges through the incorporation of precise RF-focused models and design tools.

This paper presents the case study of a real-world first-pass functional silicon success story of a highly integrated digital transceiver from Orca Systems.

This product leverages nanoscale CMOS techniques to solve real-world problems and serves as a perfect embodiment of next-generation design challenges and their reliance on accurate RF PDK for resolution.

## Orca and Fujitsu Deliver Digital RF Design

Orca Systems has developed patented methods for digital RF transceiver designs leveraging nanoscale process technology. The company can effectively combine RF and digital functionality in a single SoC on such technologies as Fujitsu 90nm low power processes, which are known to minimize fabrication cost and power consumption through size reduction.

Equally important, the digital approach simplifies the implementation of multi-mode transceivers, so that one compact SoC can handle Bluetooth, WLAN and other wireless communications. This approach opens a future path to software-defined radio.

### Process Description

Orca Systems achieved the first-pass silicon success of their digital RF transceiver with Fujitsu 90nm low power CMOS technology.

Table 1 provides a high-level description of the devices and modules available in the Fujitsu 90nm RFCMOS process. The process is based on a robust mixed-signal baseline with available RF modules such as Inductors,

<b>CMOS</b>	Standard MOSFETs (STD)	1.2V & 3.3V
	Low Leakage, High Vth MOSFETs	1.2V
	Low Vth, High Speed MOSFETs	1.2V & 3.3V
	Optional IO Transistor Voltage Level	2.5V
<b>Triple Well (DNW)</b>		<i>Optional</i>
<b>Substrate VPNP</b>		Standard
<b>Capacitors</b>	MIM Density (fF/μm <sup>2</sup> )	1.0 or 1.5
	MFC Density (fF/μm <sup>2</sup> )	1.2
	MIS (fF/μm <sup>2</sup> ) (2.5 or 3.3V)	3.45 or 2.47
<b>Varactors</b>	MOS (LV/HV)	Standard
<b>Resistors</b>	P+ Poly (Ohm/sq)	450 (Standard)
	Silicided P+ Poly (Ohm/sq)	11 (Standard)
<b>Fuse</b>	Tungsten	<i>Optional</i>
	E-fuse OTP	<i>Optional</i>
<b>Inductors</b>	Single-Ended/Differential	2x0.9μm (or 3.3μm)
<b>Metal</b>	Total Number Metal Layers	8 (8G)
	3.3μm Top Cu	Optional (7E)
	1.17μm Al RDL	Standard

**Table 1 — Fujitsu 90nm RFCMOS device description**

Varactors, and MIM capacitors. These modules are complimented by a rich set of available IPs including USB/HDMI/SATA/PCIE interfaces, ARM processor, PLL, ADC/DAC, and memories.

**PDK and Device Modeling**

To better access these technology features, Fujitsu has developed a custom process design kit (PDK) that improves design efficiency. Orca Systems leveraged this PDK to design and tape-out their first-pass functional silicon. Fujitsu's PDK includes a collection of verified data files for use by custom IC design tools. These files include schematic symbols, foundry-specific models, GDSII-layer technology files, parameterized cells (PCells), DRC/LVS runset, parasitic extraction runset and embedded scripts that automate the generation and verification of design data. Figure 1 showcases the generic RF design flow and PDK interaction.

To enable precise and flexible RF CMOS design, the PDK supports PSP transistor models as well as BSIM4

models. The PSP model belongs to a new class of transistor models developed to solve the challenges of nanoscale RF design, where they must operate across a wide range of bias conditions and estimate correctly the circuit harmonics and linearity.

As an example of device model accuracy and its proof, the proximity of the isolation trench to active MOSFET channels has been shown to impact critical analog figures of merit including threshold voltage, mobility, and saturation velocity. Common techniques to mitigate these effects include the addition of area-intensive dummy devices. The PDK's accurate STI proximity models provide the designer visibility into the induced deviations to serve as a guide in deploying counter measures such as dummy addition. An example of the stress model validation is shown in Figure 2 on the following page. In this plot statistical data on three key measurements was collected on 1.2V NFETs with varying proximity distances and compared to the PSP model.

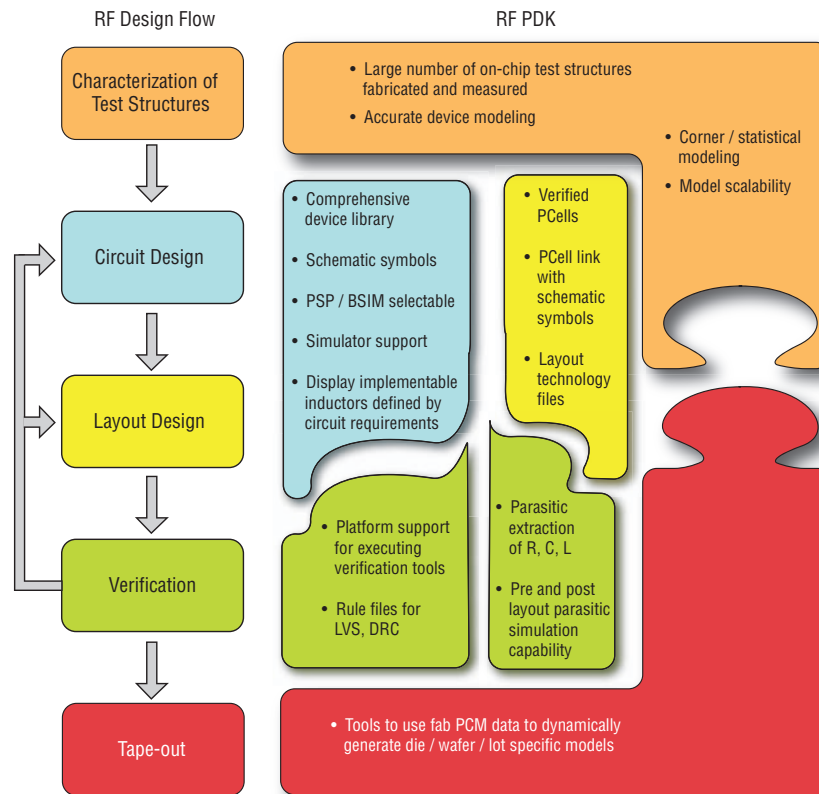


Figure 1 — The RF Process Design Kit (PDK) is integrated to support the design flow

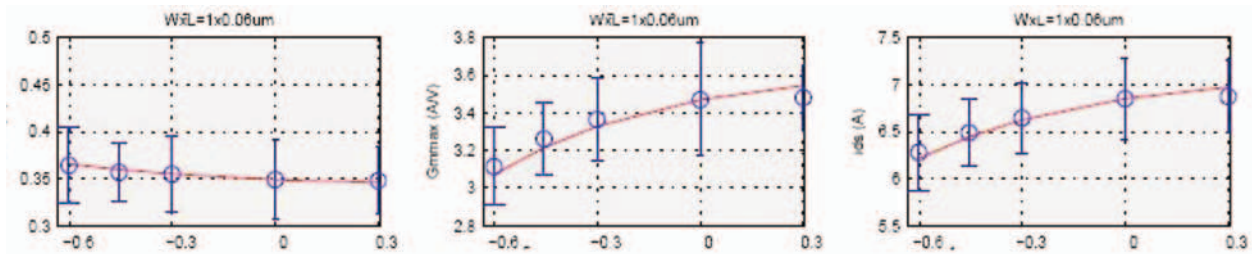


Figure 2 — 1.2V NFET stress effect model validation for threshold voltage, peak transconductance and saturation current

Finally, CMOS modeling is complimented with a rich set of RF-focused features including scalable inductor synthesis, scalable MOS varactor models, and X-sigma yield optimization tools.

**Verification Result**

The accuracy of the modeling platform is presented below by comparisons between simulated and measured data for Orca Systems' digital receiver and digital synthesizer blocks.

**Digital Receiver Design**

The digital receiver is an important circuit architecture that has been used to realize a Bluetooth transceiver and other wireless systems. The block diagram below illustrates the concept of the receiver architecture adopted by the Orca Systems digital receiver. The sampling technique with software-tunable filters is used for directly converting the RF to baseband. Noise figures of the sampling receiver are comparable to a standard analog mixer approach.

**DIGITAL RECEIVER VALIDATION RESULT**

First, the linearity of the sampler is analyzed as it is a difficult and heavily model-dependent RF simulation. Using the PDK-supplied models, excellent correspondence between simulated and measured IP3 is seen. Orca's Bluetooth Sampler's IP3 simulation results at +3 dBVrms perfectly match the +3 dBVrms measurements and serve as evidence of comprehensive accuracy.

Another key aspect in the synthesizer design is the use of a high-frequency inductor. Phase noise and center frequency accuracy are heavily dependent on the inductor Q and value accuracy. For example, if the Q is different between model and silicon, then the phase noise accuracy will suffer. Similarly, if the inductance and model are not accurate then the center frequency accuracy will suffer. After RLC extraction using the Fujitsu PDK, the error in center frequency between simulation and silicon is <4% and is within the variation predicted by statistical simulations.

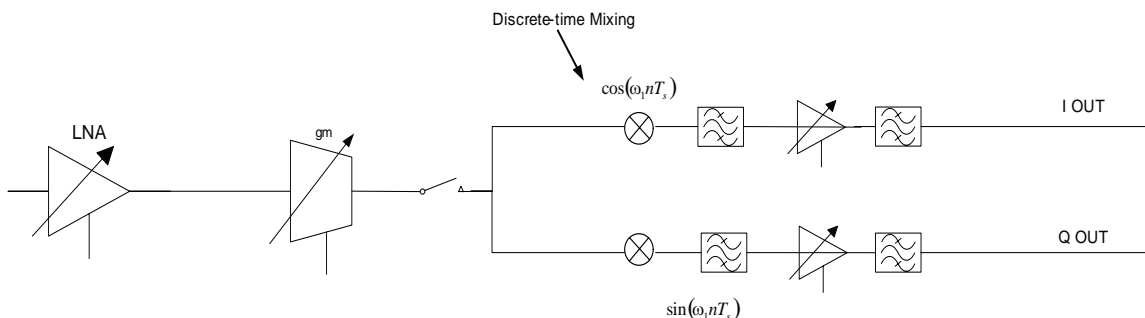
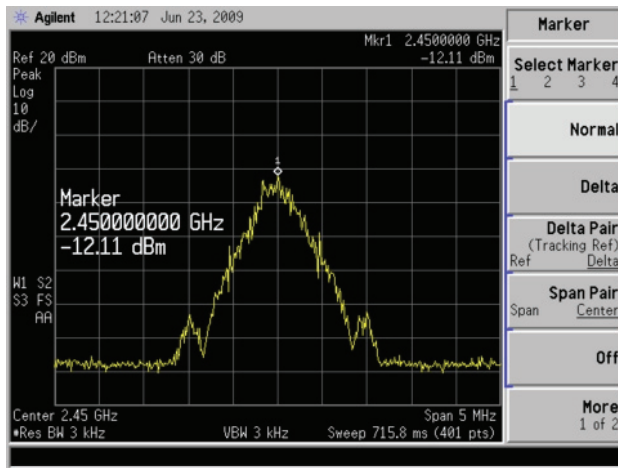


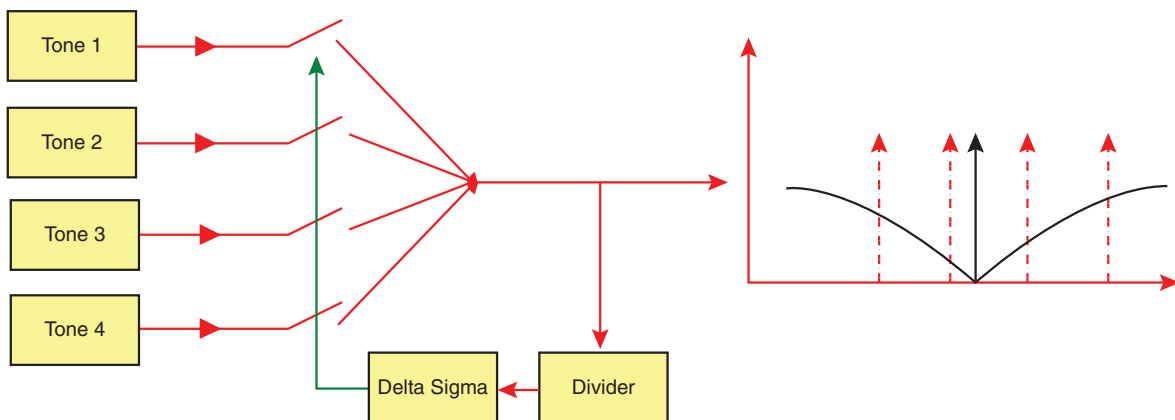
Figure 3 — Representative Diagram of Orca's digital receiver technology



**Figure 4 — Output of the DSP-RF PA when performing modulation**

Since the digital synthesizer is capable of modulation, the DSP-RF PA with modulation is tested. Figure 4 shows that the digital PA is capable of high-speed modulation for the Bluetooth application.

The result shows that the total output power of the digital PA behaves as simulated. The total channel power in the simulation is approximately +5 dBm and the silicon result (obtained from integrating the spectrum in Figure 4) is ~+4 dBm. This is typically a very difficult simulation because of the model dependence.



**Figure 5 — Orca's DSP-RF approach for generating precise high frequency reference**

### Digital Synthesizer Design

To efficiently implement the functions of the digital synthesizer in Figure 5, a new approach has been taken where the frequency synthesis process is made open-loop. Reference tones are generated and then sigma-delta averaged to produce the fractional tones hence, eliminating the need for a PLL (or ADPLL). The phase noise performance of the final output is as good as or better than that of an analog PLL.

Since the synthesizer is open-loop, this allows for very wide-band modulation without the need for an I/Q up-converter. This improves yield and reduces die size and power consumption.

### Digital Synthesizer Validation Result

Phase noise is analyzed as another example of a difficult and error-prone simulation. For Orca's DSP-RF-based synthesizer, the phase noise of individual blocks is simulated in Cadence Spectre-RF and is placed into a behavioral model to estimate the total system phase noise.

Figure 6 on the following page depicts the DSP-RF synthesizer overall phase noise profile. The x-axis is frequency and y-axis is phase noise in dBc/Hz. This is measured at the synthesizer output port (red curve) and shows a difference of +/- 1.5 dB from simulation (blue curve). In this design, a low phase noise of -119 dBc/Hz is achieved at an offset of 1MHz, showing good performance as well as simulation correspondence.

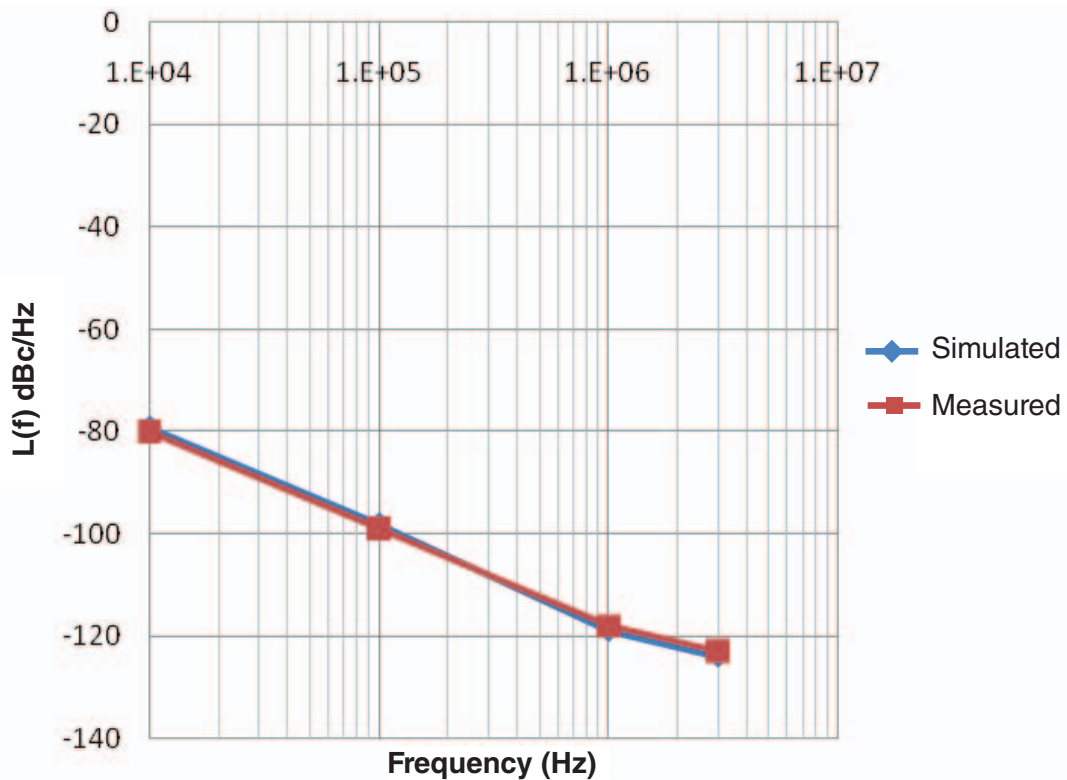


Figure 6— Synthesizer’s phase noise performance at 2.4 GHz

As with linearity, precise phase noise correspondence highlights PDK accuracy extending across device model DC, AC, RF, and noise feature sets as well as in layout parasitic extraction. The correspondence quality of these two figures substantiated Orca’s target of first-time-right function silicon.

### Conclusion

Orca’s digital transceivers were successfully designed for Bluetooth and other applications using the Fujitsu 90nm CMOS process design kit (PDK), and were verified with actual silicon measurements in good correspondence.

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Fujitsu believes this case study is a great showcase of its contribution to the first-pass functional silicon success primarily through its highly accurate modeling of circuit-level devices that is critical for precision applications such as RF.

### About Orca Systems

Founded in 2004 with locations in San Diego and Bangalore, Orca Systems offers its silicon intellectual property (IP) on a licensing basis. The company currently has customers in Japan and the US.

## FUJITSU MICROELECTRONICS LIMITED

Nomura Shin-Yokohama Bldg., 2-10-23 Shinyokohama, Kohoku-ku, Yokohama, Kanagawa 222-0033, Japan  
Tel: +81-45-755-7000 Web Site: <http://jp.fujitsu.com/fml/en/>

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